AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 2, line 8 with the following:

In the hardware design (or H/W design), elements having equivalent functions of the algorithms are generally described by equivalent HDL source code(which stands for 'Hardware Description Language'), then, composition of circuitry is carried out (see step B3). In step B4, verification is made as to whether the sources operate correct or not. In the software design (or S/W design), elements having equivalent functions of the algorithms are generally described by equivalent source code of a programming language having a CPU dependency (see step B5). In step B6, verification is made as to whether the sources operate ~~correct~~ correctly or not. Lastly, cooperative verification is performed on combinations of the hardware and software (see step B7).

Please replace the paragraph bridging pages 3 and 4 with the following paragraph:

It is an object of the invention to provide a bus performance evaluation method for algorithm description by which it is possible to considerably reduce turnaround times in design of LSI by excluding unwanted operations regarding feedback loops derived from cooperative verification in the hardware design and software design. According to an aspect of the invention, these provide a method as defined in independent claim [[1]] 11. Basically, this invention provides improvements in procedures for the design and development of LSI. That is, after isolation of the hardware and software being effected with respect to sources described by the general purpose high-level language in algorithm design, an evaluation function is created to count traffic of the bus interconnecting elements to be implemented in hardware and/or in software. The sources are modified such that the evaluation function is performed every time

data (e.g., a variable) is loaded onto the bus. Then, evaluation is performed on the performance of the bus having a processing rate. Based on the bus traffic that is finally produced with respect to the processing rate, isolation of the hardware and software is optimally performed at the prescribed stage of the architecture design. Thus, it is possible to exclude the feedback loops regarding the isolation between the hardware and software from the cooperative verification after the actual coding. As a result, it is possible to considerably reduce the turnaround time in the design of LSI.

Please replace the paragraph beginning on page 5, line 17 with the following:

FIG. 4 is a flowchart showing ~~procedures of work that are~~ a procedure that is effected by the first embodiment shown in FIG. 2;

Please replace the paragraph beginning on page 6, line 22 with the following:

Next, a simulation program ~~platform~~ is structured to perform architecture design by using sources, which are used in the aforementioned algorithm design. Namely, in the simulation platform structuring process, the flow proceeds to step A3 to effect isolation of the hardware and software. In step A4, an evaluation function is created. Herein, it is satisfactory that the evaluation function has an operation of counting a certain value.

Please replace the paragraphs beginning on page 7, line 3 with the following:

In step A5, variables loaded onto the bus interconnecting between the hardware and software are being selected. Then, the flow proceeds to step A6 in which sources that are used in the algorithm design are modified by executing the created evaluation function when data are written to the variables loaded onto the bus, in other words, when data transfer is effected on the bus that is a subject of evaluation (hereinafter, simply referred to as the 'evaluated' bus). In

response to modifications of the sources, the simulation ~~platform~~ program for use in the architecture design is structured again.

Please replace the paragraph beginning on page 7, line 19 with the following:

Using the bus traffic that is calculated in response to the processing rate, it is possible to check validity with respect to isolation of the hardware and software and a bus configuration. If the validity check causes a change of the bus, the sources that are described by the general purpose high-level language such as the C language and C++ language are modified, then, the simulation ~~platform~~ program is structured again and the performance evaluation is performed again. That is, the present procedures provide a feedback loop (see step A16) for feeding back the result of the performance evaluation of the bus. Due to provision of such a feedback loop, it is possible to actualize the architecture design at the high-level stage of design.

Please replace the paragraph beginning on page 9, line 22 with the following:

FIG. 3 shows an example of the 'restructured' simulation platform. With reference to the restructured simulation ~~platform~~ program shown in FIG. 3, the variable b is regarded as one that is not to be loaded onto the evaluated bus because of result of the performance evaluation of the bus. That is, the restructured simulation ~~platform~~ has only two variables a, b that are being loaded onto the evaluated bus. Since the variable b is not loaded onto the bus, the evaluation function BUS0() is not embedded subsequent to the variable b to which data is written. In contrast, the evaluation function BUS0() is certainly embedded subsequent to the variables a, c to which data are written respectively. Thus, the evaluation function BUS0() is certainly executed just after the variables a, c to which the data are written respectively.

Please replace the paragraph beginning on page 10, line 7, with the following:

After restructuring of the simulation ~~platform~~ program, verification is performed by simulation. Then, the bus traffic for the processing rate is calculated again in accordance with the equation (1), so that evaluation is to be performed on the performance of the bus.

Please replace the paragraph beginning on page 10, line 11, with the following:

Through the aforementioned operations, an average bus traffic is produced with respect to the data rate of the evaluated bus. Then, performance evaluation is performed on the bus, so that the result of the performance evaluation is fed back to structuring of the simulation ~~platform~~ program. Hence, it is possible to actualize the architecture design at the high-level stage of design

Please replace the paragraph beginning on page 11, line 5 with the following:

In step C5, a decision is made as to whether description of the sources reading in the aforementioned works is completed up to the last line of the sources originally used in the algorithm design or not. Thus, modification is effected on the sources originally used in the algorithm design. After the modification proceeds to the last line of the sources used in the algorithm design, the flow proceeds to step C6 in which the system compiles the modified sources to structure the simulation ~~platform~~ program for use in the architecture design. In step C7, bus traffic is calculated for the evaluated bus by execution of the simulation ~~platform~~ program~~-~~. Because the processing rate requested by the main function is already known, the bus traffic for the processing rate is produced so that performance evaluation is performed on the

evaluated bus in step C8.

Please replace the paragraph beginning on page 16, line 24 with the following paragraph:

FIG. 10 shows an example of a simulation ~~platform~~ program that is structured by sources described by the C++ language.

Please replace the paragraph beginning on page 17, line 17 with the following paragraph:

Different from the foregoing embodiments (including the first embodiment of FIG. 2), the simulation ~~platform~~ program of FIG. 10 is characterized by the sources being described by the C++ language. To perform performance evaluation on the bus, bus traffic for its processing rate is calculated by the aforementioned equation (1).

Please replace the paragraph beginning on page 17, line 21 with the following paragraph:

Although the simulation ~~platform~~ program is structured using the sources described by the C++ language as shown in FIG. 10, it proceeds to calculation of the bus traffic for the processing rate and performance evaluation of the bus, then, it feeds back the result of the performance evaluation to restructuring of the simulation ~~platform~~ program. Therefore, it is possible to carry out the architecture design at the high-level stage of design

Please replace the paragraph beginning on page 18, line 1 with the following paragraph:

As described heretofore, this invention is designed such that when data transfer is caused on the bus interconnecting between the hardware and software to be evaluated, the sources that are used in the architecture design and are described by the general purpose high-level language such as the C language and C++ language are modified by executing the specific evaluation function, so that the simulation ~~platform~~ program for use in the architecture design is structured. Then, simulation is performed using the structured simulation ~~platform~~ program to calculate the bus traffic for the processing rate of the evaluated bus. Thus, it is possible to perform the bus performance evaluation at the high-level stage of design.

Please replace the paragraph beginning on page 19, line 11 with the following paragraph:

Because the architecture design is performed using the sources that are described by the general purpose high-level language, it is possible to simplify feedback procedures due to the architecture design. By optimally performing isolation of the hardware and software at the prescribed stage of the architecture design, it is possible to exclude feedback loops regarding the isolation of the hardware and software from the cooperative verification after the actual coding. This guarantees considerable reduction of the turnaround time of design. As compared with the HDL and assembly languages, the C and C++ ~~language~~ languages can be used with a relatively ~~relative~~ small number of lines of code. That is, those languages can be easily changed and modified according to needs.